AMENDMENTS

In The Claims

Claim 1. (currently amended) A PFC-PWM controller of a power converter having interleaved switching, comprising:

a PFC stage, for generating a PFC signal in response to ~~the~~ a line input voltage and a first feedback voltage;

a PWM stage, for generating a PWM signal in response to a second feedback voltage;

a power manager, for generating a discharge current and a burst-signal;

an oscillator, for generating a ramp-signal, a slope-signal and a pulse-signal;

an ON/OFF signal, for turning the power converter on and off; and

a sequencer, for generating a first enable-signal to control said PFC signal, and a second enable-signal to control said PWM signal.

Claim 2. (currently amended) The PFC-PWM controller of claim **1**, wherein said PFC signal is used to control a PFC boost converter of said power converter, wherein said first feedback voltage is derived from ~~the~~ a PFC boost converter feedback loop, wherein said first feedback voltage decreases whenever ~~the~~ a load of ~~the~~ said power converter decreases, wherein ~~the magnitude of~~ said first feedback voltage decreases whenever ~~the magnitude of the~~ an output voltage of ~~the~~ said PFC boost converter increases.

Claim 3. (currently amended) The PFC-PWM controller of claim **1**, wherein said PWM signal is used to control a DC-to-DC ~~power~~ converter of said power converter, wherein said second feedback voltage is derived from ~~the~~ a DC-to-DC ~~power~~ converter feedback loop,

wherein ~~the magnitude of~~ said second feedback voltage decreases whenever ~~the~~ said load of ~~the~~ said power converter decreases, wherein ~~the magnitude of~~ said second feedback voltage increases whenever ~~the magnitude of the~~ said output voltage of ~~the~~ said DC-to-DC ~~power~~ converter increases.

Claim 4. (currently amended) The PFC-PWM controller of claim 1, wherein ~~the amplitude of~~ said discharge current decreases whenever ~~the magnitude of~~ said first feedback voltage decreases below ~~the magnitude of~~ a first green-threshold voltage, wherein ~~the amplitude of~~ said discharge current will decrease proportionally to ~~the magnitude of~~ said first feedback voltage, wherein ~~the amplitude of~~ said discharge current decreases whenever ~~the magnitude of~~ said second feedback voltage decreases below ~~the magnitude of~~ a second green-threshold voltage, wherein ~~the amplitude of~~ said discharge current will decrease proportionally to ~~the magnitude of~~ said second feedback voltage, wherein said discharge current mirrors a green-current, wherein a green-voltage is produced in response to said discharge current.

Claim 5. (currently amended) The PFC-PWM controller of claim 1, wherein said burst-signal is utilized to disable said PFC signal, wherein disabling said PFC signal makes the PFC-PWM controller enter a suspended state, wherein said green-voltage is compared with a first threshold voltage, wherein whenever said green-voltage decreases below said first threshold voltage, the PFC-PWM controller will enter a low-load state, wherein whenever ~~the~~ a duration of said low-load state exceeds a first delay-time, the PFC-PWM controller will enter said suspended state, wherein said burst-signal is ~~disable~~ disabled whenever said first feedback voltage exceeds a second threshold voltage while the PFC-PWM controller is in said suspended state.

Claim 6. (currently amended) The PFC-PWM controller of claim **1**, wherein said ramp-signal and said slope-signal are synchronized with said pulse-signal, wherein said pulse-signal is inserted between said PFC signal and said PWM signal, wherein ~~the~~ a rising-edge of said pulse-signal disables said PFC signal, wherein ~~the~~ a falling-edge of said pulse-signal enables said PWM signal, wherein ~~the~~ a pulse width of said pulse-signal increases whenever ~~the amplitude of~~ said discharge current decreases.

Claim 7. (original) The PFC-PWM controller of claim **1**, wherein said PFC signal is generated by comparing said first feedback voltage with said slope-signal, wherein said PWM signal is generated by comparing said second feedback voltage with said ramp-signal.

Claim 8. (currently amended) The PFC-PWM controller of claim **1**, wherein said sequencer enters a no-brownout state whenever ~~the~~ said line input voltage exceeds a third threshold voltage, wherein said sequencer transits from said no-brownout state to a first state when ~~the~~ said no-brownout condition is sustained longer than a second delay-time, wherein said sequencer transits from said first state to a second state as said ON/OFF signal is enabled, wherein said sequencer transits from said second state to a third state when said second state is sustained longer than a third-delay time, wherein said first enable-signal will be logic-high whenever said sequencer is in the third state while said burst-signal is disabled, wherein said sequencer transits from said third state to a fourth state whenever said first feedback voltage exceeds a fourth threshold voltage, which indicates a PFC-ready condition, wherein said sequencer transits from said fourth state to a fifth state whenever said fourth state is sustained

longer than a fourth delay-time, wherein said second enable-signal will be logic-high whenever said sequencer is in said fifth state.

Claim 9. (currently amended) The PFC-PWM controller as claimed in claim **1**, wherein ~~the~~ said pulse width of said pulse-signal ensures a dead time after said PFC signal is turned off and before said PWM signal is turned on, wherein ~~the~~ said pulse width of said pulse-signal further determines ~~the~~ a maximum duty cycle of said PFC signal and said PWM signal, wherein ~~the~~ said pulse width of said pulse-signal increases and ~~the~~ a frequency of ~~the~~ said pulse-signal decreases whenever said discharge current decreases.

Claim 10. (currently amended) The PFC-PWM controller as claimed in claim **1**, wherein said power manager comprises:

a pm current source, for limiting ~~the~~ a maximum magnitude of said discharge current;

a first pm V-I converter, having a first pm ~~operation~~ operational amplifier, a first pm n-transistor, and a first pm resistor, wherein said first pm V-I converter generates a first pm current in response to said first feedback voltage whenever said first feedback voltage exceeds a first reference voltage;

a second pm V-I converter, having a second pm ~~operation~~ operational amplifier, a second pm n-transistor, and a second pm resistor, wherein said second pm V-I converter generates a second pm current in response to said second feedback voltage whenever said second feedback voltage exceeds a second reference voltage;

a first pm current mirror, consisting of a first pm p-transistor, a third pm p-transistor, and a fifth pm p-transistor, wherein ~~the~~ sources of said first, third and fifth pm p-transistors are

connected to said pm current source, wherein ~~the~~ gates of said first, third and fifth pm p-transistors are connected to a drain of said first pm p-transistor, wherein ~~said~~ a first pm current drives said drain of said first pm p-transistor and produces a first discharge current via a drain of said third pm p-transistor, wherein said first pm current drives said drain of said first pm p-transistor and produces a first green-current via a drain of said fifth pm p-transistor;

a second pm current mirror, consisting of a second pm p-transistor, a fourth pm p-transistor, and a sixth pm p-transistor, wherein ~~a source~~ sources of said second, fourth and sixth pm p-transistors are connected to said pm current source, wherein ~~a gate~~ gates of said second, fourth and sixth pm p-transistors are connected to a drain of said second pm p-transistor, wherein ~~said~~ a second pm current drives said drain of said second pm p-transistor and produces a second discharge current via a drain of said fourth pm p-transistor, wherein said second pm current ~~drives said drain of said second pm p-transistor and produces~~ further mirrors a second green-current via a drain of said sixth pm p-transistor, wherein said first discharge current and said second discharge current are coupled together to produce said discharge current;

a green-resistor, for generating said green-voltage, wherein said first green-current and said second green-current are supplied to a first terminal of said green-resistor, wherein a second terminal of said green-resistor is connected to ~~the~~ a ground reference;

a pm comparator, for comparing said green-voltage with a first threshold voltage, wherein a positive input of said pm comparator is supplied with said first threshold voltage and a negative input of said pm comparator is connected to said first terminal of said green-resistor;

a first delay-timer, for producing a first delay-time, wherein said first delay-timer has an input connected to an output of said pm comparator;

an inhibit hysteresis comparator, for comparing said first feedback voltage with a second threshold voltage, wherein a negative input of said inhibit hysteresis comparator is supplied with said first feedback voltage and a positive input of said inhibit hysteresis comparator is supplied with said second threshold voltage; and

a pm AND gate, for outputting said burst-signal, wherein an output of said first delay-timer and an output of said inhibit comparator are respectively connected to two inputs of said pm AND gate.

Claim 11. (currently amended) The PFC-PWM controller as claimed in claim 1, wherein said oscillator comprises:

an osc current source, for producing a ramp-charge current and a slope-discharge current;

a first osc current mirror, consisting of a first osc n-transistor, a second osc n-transistor, and a third osc n-transistor, wherein ~~a source~~ sources of said first, second and third osc n-transistors are connected to ~~the~~ said ground reference, wherein ~~a gate~~ gates of said first, second and third osc n-transistors are connected to a drain of said first osc n-transistor, wherein said osc current source drives ~~a~~ said drain of said first osc n-transistor and produces said slope-discharge current via a drain of said second osc n-transistor, wherein said osc current source drives said drain of said first osc n-transistor and produces a mirrored osc current via said third osc n-transistor;

a slope-charge switch, for generating said slope-signal, wherein said slope-charge switch is connected in series with a slope-discharge switch, wherein said slope-charge switch and said slope-discharge switch are controlled to alternately conduct, wherein a ~~VH~~ high-reference voltage is supplied to a first terminal of said slope-charge switch, wherein a second terminal of said slope-discharge switch is connected to said drain of said second osc n-transistor;

a slope capacitor, for generating said slope-signal, wherein said slope capacitor is connected to ~~the~~ a junction of said slope-charge switch and said slope-discharge switch, wherein said slope capacitor is rapidly charged up to said ~~VH~~ high-reference voltage whenever ~~the~~ said slope-charge switch is turned on, wherein said slope capacitor is rapidly discharged by said slope-discharge current whenever said slope-discharge switch is turned on;

a second osc current mirror, consisting of a first osc p-transistor and a second osc p-transistor, wherein ~~the~~ sources of ~~these two~~ said first and second osc p-transistors are supplied with ~~the~~ a voltage source, wherein ~~the~~ gates of said first and second osc p-transistors are connected to a drain of said first osc p-transistor; wherein said mirrored osc current drives said drain of said first osc p-transistor and produces a ramp-charge current via a drain of said second osc p-transistor;

a third osc current mirror, consisting of a fourth osc n-transistor and a fifth osc n-transistor, wherein ~~the~~ sources of said fourth and fifth osc n-transistors are connected to ~~the~~ said ground reference, wherein ~~the~~ gates of said fourth and fifth osc n-transistors are connected to a drain of said fourth osc n-transistor, wherein said discharge current drives said drain of said

fourth osc n-transistor and produces a ramp-discharge current via a drain of said fifth osc n-transistor;

a ramp-charge switch and a ramp-discharge switch, for generating said ramp-signal, wherein said ramp-charge switch is connected in series with said ramp-discharge switch, wherein said ramp-charge switch and said ramp-discharge switch are controlled to alternately conduct, wherein said ramp-charge current is supplied to a first terminal of said ramp-charge switch, wherein a second terminal of said ramp-discharge switch is connected to a drain of said fifth osc n-transistor;

a ramp capacitor, for generating ~~the~~ said ramp-signal, wherein said ramp capacitor is connected to ~~the~~ a junction of said ramp-charge switch and said ramp-discharge switch, wherein said ramp capacitor is charged up by said ramp-charge current whenever said ramp-charge switch is turned on, wherein said ramp capacitor is discharged by said ramp-discharge current whenever said ramp-discharge switch is turned on;

a high-side comparator and a low-side comparator, wherein ~~the~~ negative inputs of said high-side comparator and said low-side comparator are connected to said ramp capacitor, wherein a positive input of said high-side comparator is supplied with said ~~VH~~ high-reference voltage, wherein a positive input of said low-side comparator is supplied with a ~~VL~~ low-reference voltage;

a first NAND gate and a second NAND gate, wherein said pulse-signal is generated at an output of said first NAND gate, wherein said output of said first NAND gate is connected to a second input of said second NAND gate, wherein an output of said second NAND gate is

connected to a second input of said first NAND gate, wherein a first input of said first NAND gate is connected to an output of said high-side comparator, wherein a first input of said second NAND gate is connected to an output of said low-side comparator; and

an osc inverter, for generating an inverse pulse-signal, wherein an input of said osc inverter is connected to said output of said first NAND gate, wherein said pulse-signal is utilized to enable said ramp-discharge switch and said slope-charge switch, wherein said inverse pulse-signal is applied to enable said ramp-charge switch and said slope-discharge switch.

Claim 12. (currently amended) The PFC-PWM controller as claimed in claim **1**, wherein said sequencer comprises:

a first sq comparator, for comparing ~~the~~ said line input voltage with a third threshold voltage, wherein a positive input of said first sq comparator is supplied with ~~the~~ said line input voltage, wherein a negative input of said first sq comparator is supplied with said third threshold voltage, wherein said first sq comparator is used to transit said sequencer into ~~said~~ a first state;

a second delay-timer, for determining a second-delay time, wherein an input of said second delay-timer is connected to an output of said first sq comparator;

a first sq AND gate, for transiting said sequencer into ~~said~~ a second state, wherein a first input of said first sq AND gate is supplied with said ON/OFF signal, wherein a second input of said first sq AND gate is connected to an output of said second delay-timer;

a third delay-timer, for determining a third delay-time and transiting said sequencer into ~~said~~ a third state, wherein an input of said third delay-timer is connected to an output of said first sq AND gate;

a sq inverter, having an input supplied with said burst-signal;

a second sq AND gate, for producing said first enable-signal, wherein a first input of said second sq AND gate is connected to an output of said sq inverter, wherein a second input of said second sq AND gate is connected to an output of said third delay-timer;

a second sq comparator, for comparing said first feedback voltage with a fourth threshold voltage, wherein said second sq comparator indicates ~~said~~ a PFC-ready condition; wherein a positive input of said second sq comparator is supplied with said first feedback voltage, wherein a negative input of said second sq comparator is supplied with said fourth threshold voltage;

a third sq AND gate, for transiting said sequencer into ~~said~~ a fourth state, wherein a first input of said third sq AND gate is connected to said output of said third delay-timer, wherein a second input of said third sq AND gate is connected to an output of said second sq comparator; and

a fourth delay-timer, for producing a fourth delay-time and transiting said sequencer into ~~said~~ a fifth state, wherein an input of said fourth delay-timer is connected to an output of said third sq AND gate, wherein said second enable-signal is logic-high whenever said sequencer is in said fifth state.

Claim 13. (currently amended) The PFC-PWM controller as claimed in claim **1**, wherein said PFC stage comprises:

a pfc comparator, for comparing said first feedback voltage with said slope-signal, wherein a positive input of said pfc comparator is supplied with said first feedback voltage and a negative input of said pfc comparator is supplied with said slope-signal;

a first pfc inverter, having an input supplied with said pulse-signal;

a second pfc inverter, having an input supplied with a first protection signal;

a first pfc AND gate having a first input connected to an output of said first pfc inverter, said first pfc AND gate having a second input connected to an output of said second pfc inverter;

a first pfc flip-flop and a second pfc flip-flop, for producing said PFC signal at an output of said second pfc flip-flop, wherein ~~the~~ D-inputs of said first pfc flip-flop and said second pfc flip-flop are supplied with said first enable-signal, wherein a clock-input of said second pfc flip-flop is connected to an output of said first pfc flip-flop, wherein a reset-input of said first pfc flip-flop is connected to said output of said first pfc inverter, wherein a reset-input of said second pfc flip-flop is connected to an output of said first pfc AND gate;

a delay circuit, having an input connected to said output of said first pfc inverter; and

a second pfc AND gate, having two inputs respectively connected to an output of said pfc comparator and to an output of said delay circuit, wherein an output of said second pfc AND gate is connected to a clock-input of said first pfc flip-flop.

Claim 14. (currently amended) The PFC-PWM controller as claimed in claim 1, wherein said PWM stage comprises:

a first pwm comparator, for comparing said second feedback voltage with said ramp-signal, wherein a positive input of said first pwm comparator is supplied with said second feedback voltage, and a negative input of said first pwm comparator is supplied with said ramp-signal;

a first pwm inverter, having an input supplied with said pulse-signal;

a second-pwm inverter, having an input supplied with a second protection signal;

a first pwm AND gate, having two inputs respectively connected to an output of said first pwm comparator and an output of said second pwm inverter;

a first pwm flip-flop and a second pwm flip-flop, wherein ~~the~~ D-inputs of said first pwm flip-flop and said second pwm flip-flop are supplied with said second enable-signal, wherein ~~the~~ clock-inputs of said first pwm flip-flop and said second pwm flip-flop are connected to an output of said first pwm inverter, wherein a reset-input of said first pwm flip-flop is connected to an output of said first pwm AND gate;

a second pwm comparator, for comparing a fifth threshold voltage with said ramp-signal and determining ~~the~~ a maximum duty cycle of said PWM signal, wherein a positive input of said second pwm comparator is supplied with said fifth threshold voltage, wherein a negative input of said second pwm comparator is supplied with said ramp-signal, wherein an output of said second pwm comparator is connected to a reset-input of said second pwm flip-flop; and

a second pwm AND gate, for generating said PWM signal, wherein a first input of said second pwm AND gate is connected to an output of said first pwm flip-flop, wherein a second input of said second pwm AND gate is connected to an output of said second pwm flip-flop, wherein a third input of said second pwm AND gate is connected to ~~an~~ said output of said first pwm inverter.